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The EDA Chokepoint Dilemma? Openness, Oligopolies, and China's Ecosystem

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Abstract

One of the fiercest domains of U.S.-China technology rivalry centers around semiconductors, which enable advances in a range of strategic and essential sectors—from communications and computing, to healthcare, military systems, and transportation. For policymakers interested in stymying Chinese advances in semiconductors, the perfect chokepoint to exploit through export restrictions is a product that plays an indispensable role in the broader ecosystem and is controlled by very few companies with high market-entry barriers. This paper reviews experience with one such product: electronic design automation (EDA) tools. The author argues that the U.S. and allied governments can use EDA as a chokepoint to curb China's chip design capabilities in the medium term, but that they should also strengthen incentives for the development and adoption of open-source EDA tools by the broader industry. Supporting the development of open-source EDA tools does not diminish their market dominance at the cutting-edge but "democratizes" chip design at the trailing-edge and mature nodes—of high relevance for industrial, automotive, and health applications.

Keywords: Technology, geopolitics, economic security, export controls

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Introduction

The U.S.-China technology rivalry has largely centered around semiconductors for the last couple of years. In search of "chokepoints," the U.S. government goes, sometimes in unison with allied governments, through the semiconductor value chain—from products (chips) to manufacturing equipment, chemicals, and raw materials to wafers and design software. For policymakers, the perfect chokepoint to exploit through export restrictions is a product that plays an indispensable role in the broader ecosystem and is controlled by very few, ideally one, companies with high market-entry barriers. The best-known example is Extreme-Ultra-Violet (EUV) steppers from Dutch equipment manufacturer ASML. Without access to EUV lithography machines, a semiconductor manufacturer cannot advance beyond 7 nm process technology. It took ASML and its 5,000 suppliers (of which roughly 200 are considered "critical") the better part of two decades to develop these machines.

Not allowing EUV machines to enter the Chinese market (through export restrictions based on the multilateral Wassenaar Arrangement) curbs China's semiconductor manufacturing capabilities for the foreseeable future at around 7 nm. It is highly unlikely that Chinese companies would be able to (a) reverse engineer ASML's EUV steppers or (b) develop competitive alternatives through Chinese companies such as Shanghai Micro Electronics Equipment Group (SMEE) within this decade.[1] China would need to replicate an entire ecosystem of highly specialized component suppliers, such as German ZEISS (optics, lenses) or TRUMPF (laser light source). For China, it is thus not just about substituting an export-controlled technology but first building the ecosystem necessary to advance and sustain indigenous innovation and commercialization.

Over the past years, more supposed chokepoints in semiconductor technologies have been identified and utilized through uni- and multilateral export restrictions to curb China's technological advancements. Most recently the U.S. government released a swath of new export controls on October 7, 2022, intended to "freeze" China's capabilities in a variety of semiconductor technologies, such as supercomputing, artificial intelligence (AI), front-end manufacturing, and semiconductor manufacturing equipment (SME).[2] Other examples are restrictions on top-of-the-line AI accelerators from Nvidia and AMD[3] and restrictions on electronic design automation (EDA) tools

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1 Ivan Platonov and Xwen Zheng. 2021. "Deep Dive: SMEE and China's Attempt to Replace ASML Tools." https://equalocean.com/analysis/2021062316392

2 Reva Goujon, Lauren Dudley, Jan-Peter Kleinhans, and Agatha Kratz. 2022. "Freeze-in-Place: The Impact of US Tech Controls on China". Rhodium Group. https://rhg.com/research/freeze-in-place/

3 Cheng Ting-Fang. 2022. "U.S. tightens chip export rules to China, hitting Nvidia and AMD." Nikkei Asia. https://asia.nikkei.com/Business/Tech/Semiconductors/U.S.-tightens-chip-export-rules-to-China-hitting-Nvidia-and-AMD

capable of designing circuits based on Gate-All-Around Field-Effect Transistors (GAAFET)[4]—the next-generation transistor architectures necessary to achieve feature sizes smaller than 3 nm. Some U.S. politicians even argue that all EDA software should be designated as a Foundational Technology forcing U.S. EDA suppliers such as Synopsys, Cadence Design Systems, and Mentor Graphics (Siemens EDA) to get a license from the U.S. Bureau of Industry and Security (BIS) for any sales to China.[5]
This paper argues that the U.S. and allied governments can utilize EDA as a chokepoint to curb China's chip design capabilities in the medium term. But such a strategy should not keep policymakers from also incentivizing the development and adoption of *open-source* EDA tools by the broader industry. Such a two-pronged strategy may seem counter-intuitive and contradictory at first glance: For export controls to work, the EDA market would need to remain a U.S.-based oligopoly—as has been the case for the past 20 years. Supporting the development of open-source EDA tools does not diminish their market dominance at the cutting-edge but "democratizes" chip design at the trailing-edge and mature nodes, which are of high relevance for industrial, automotive, and health applications. Thus, when looking at the EDA ecosystem policymakers need to differentiate between (1) the EDA ecosystem at the cutting-edge and (2) at the trailing-edge and mature nodes.

(1) By utilizing EDA as a chokepoint through export restrictions, the U.S. government needs the EDA market for cutting-edge chip design to continue to be an oligopoly of three U.S. companies. While controlling the export of EDA tools to China incentivizes the Chinese semiconductor industry to establish domestic competitors, it is highly unlikely that Chinese indigenous competitors for cutting-edge EDA tools will emerge within this decade—especially considering the U.S. export controls from October 7. That said, for specific steps in the design flow or specific types of chips, it is highly likely that there will be Chinese alternatives to U.S. EDA incumbents in the short to medium term. The reason for that is China's increasingly competitive foundries, fabless, and system companies (hyperscalers, automotive, consumer electronics, mobile infrastructure), growing the total addressable market for Chinese EDA suppliers. This does not mean, however, that there will be a viable Chinese competitor to the three U.S. incumbents within this decade able to offer solutions for the entire design process flow, let alone for cutting-edge front-end manufacturing.

(2) Incentivizing the development and adoption of an *open-source* EDA ecosystem will not negatively impact the, almost certain, continued dominance of U.S. incumbent EDA tool suppliers for cutting-edge chip designs. Counter-intuitively, the U.S. and allied

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[4] BIS. 2022. "Implementation of Certain Wassenaar Arrangement Decisions on Four Technologies." https://www.regulations.gov/document/BIS-2022-0006-0001

[5] See letter from Senator Tom Cotton and Member of Congress Michael McCaul to US Department of Commerce: https://www.cotton.senate.gov/imo/media/doc/edaletter.pdf

governments can do two things at the same time: ensure and exploit the oligopoly of U.S. EDA suppliers to curb China's technological advances at the cutting-edge and lower the barriers to entry for chip design at the trailing-edge and mature nodes to spark innovation across a variety of sectors. The latter would be crucial for long-term competitiveness because EDA plays a critical role in the semiconductor ecosystem as the enabling technology to design chips. The easier it is to access and work with EDA tools and the more powerful they are, the easier it is (in terms of financial and human resources) to design chips. This is not just true for academics and startups but also the military, which is why Defense Advanced Research Projects Agency (DARPA) invested hundreds of millions of U.S. dollars in open-source EDA tools as part of its Electronics Resurgence Initiative.[6] Thus, incentivizing the development of open-source EDA tools to lower barriers of entry to chip design holds significant potential for long-term innovation within the U.S. chip design ecosystem.

To explain how U.S. and allied policymakers can do both at the same time—supporting an EDA oligopoly at the cutting-edge and incentivizing the development of an open-source EDA tool ecosystem at the trailing-edge—the paper will provide a brief overview of the global EDA ecosystem and the role that EDA plays in semiconductor manufacturing. The next section will then look at the rise of Chinese EDA companies and draw connections to China's foundry and chip design ecosystem. The following section discusses two long-term trends in EDA. The last section concludes with an assessment of the two aforementioned incentives and why only restricting the export of EDA tools without a continued investment in open-source EDA tools might be detrimental to the long-term competitiveness of U.S. chip design capabilities.

The critical role of electronic design automation (EDA)

Electronic design automation (EDA) plays a crucial role in the semiconductor ecosystem because it does not simply enable chip design but creates the link to front-end and back-end manufacturing. Nonetheless, with $13 billion revenue in 2021, the global EDA market, including semiconductor intellectual property (IP), is small.[7] For comparison, in 2021 manufacturing equipment sales as well as global foundry (semiconductor contract

[6] DARPA. 2018. Electronics Resurgence Initiative. https://www.darpa.mil/work-with-us/electronics-resurgence-initiative

[7] SEMI. 2022. "Electronic System Design Industry Logs 14.4% Year-Over-Year Revenue Growth in Q4 2021, ESD Alliance Reports." https://www.semi.org/en/news-media-press-releases/semi-press-releases/electronic-system-design-industry-logs-14.4%25-year-over-year-revenue-growth-in-q4-2021-esd-alliance-reports

manufacturing) sales were each more than $100 billion.[8] For more than two decades the EDA market (without semiconductor IP) accounted for roughly 2 percent of global semiconductor revenue.

With increasing specialization and customization of chips over the years, the chip design workflow simultaneously advanced in its complexity. Importantly, the chip design flow and its various critical steps differ between different types of chips, such as mobile system-on-a-chip (SoC), memory chips, power, or analog semiconductors.
EDA is also closely interlinked with several production and process steps along the semiconductor value chain. Especially for modern processors and SoCs, third-party semiconductor IP plays a crucial role to lower complexity and time to market by utilizing pre-built functionality (such as memory or I/O) from IP vendors.[9] This explains why EDA suppliers are also important IP vendors. Additionally, since a chip design is always based on a specific process node from a specific fab, such as Taiwan Semiconductor Manufacturing Company (TSMC) N5 or Samsung 3GAP, EDA suppliers must closely collaborate with foundries to precisely simulate and verify process nodes in their software. To do that, foundries provide EDA suppliers with process development kits (PDKs)—sets of design rules and physical characteristics of a specific process technology that chip designers must adhere—that are implemented by EDA suppliers in their software tools.

In a nutshell, EDA tool suppliers have to constantly improve the different chip design process steps to enable the design of increasingly complex chips—from logic synthesis to verification and floor planning. They develop semiconductor IP and closely collaborate with fabs on new process nodes. This explains why EDA suppliers typically spend more than 35 percent of revenues on research and development—the highest research and development margin in the semiconductor industry.

The global EDA market

The EDA market is highly concentrated. The three leading EDA suppliers—Synopsys (United States, >16,000 employees), Cadence Design Systems (United States, >9,000 employees), and Mentor Graphics (Siemens EDA)[10] (United States, >6,000 employees)—

[8] SEMI. 2022. "2021 Global Semiconductor Equipment Sales Surge 44% To Industry Record $102.6 Billion, Semi Reports." https://www.semi.org/en/news-media-press-releases/semi-press-releases/2021-global-semiconductor-equipment-sales-surge-44%25-to-industry-record-%24102.6-billion-semi-reports ; EETimes. 2022. "Foundry's 31% Growth in 2021 Outpaced Overall Chip Industry." https://www.eetimes.com/foundrys-31-growth-in-2021-outpaced-overall-chip-industry/

[9] Paul McLellan. 2021. "A Brief History of Semiconductor IP." Cadence Blog. https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/iphistory

[10] Mentor Graphics was bought by German Siemens in 2017 and is now called Siemens EDA.

control more than 75 percent of global revenues.[11] Importantly, these are also the only companies whose software covers the entire design flow across all types of chips and process steps. That said, because of increasingly complex chip designs and more than 40 individual steps in the design process, companies designing chips regularly "mix and match" various EDA tools.[12] This makes it possible for smaller EDA suppliers to focus on (a) specific steps in the design flow, such as simulation, floor planning, or verification or (b) on specific types of chips, such as 3D NAND or analog semiconductors.

The dominant position of the "big three" and the resulting oligopolistic market structure are not a new development but a defining characteristic for roughly two decades.[13] This is also reflected in the business strategy of Synopsys, Cadence Design Systems (Cadence), and Mentor Graphics (Mentor): Each constantly acquires smaller companies. Synopsys alone acquired more than 100 companies, business units, or technologies so far.[14] **It is likely that the EDA market will stay an oligopoly, especially at the cutting-edge, for the following reasons**:

> **Economies of scale:** Due to the high research costs and constant pressure to innovate, EDA suppliers depend on economies of scale. This is also the reason why (a) smaller EDA suppliers and EDA startups typically only focus on specific design steps or types of chips and (b) why the "big three" EDA suppliers were so successful in their aggressive acquisition strategies.
>
> **High switching costs**: Another barrier to entry for new EDA suppliers is the reluctance of engineers to learn a new program from scratch. This is not special to EDA software but a common problem for new players to enter highly complex and specialized software markets.
>
> **Overhead for fabs**: From the perspective of foundries, an oligopoly might be preferable. EDA suppliers closely collaborate with foundries to ensure that a new process technology is precisely represented in software to be able to simulate and verify chip performance and features during the design phase.[15]

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11 TrendForce. 2022. "New US EDA Software Ban May Affect China's Advanced IC Design, Says TrendForce." https://www.trendforce.com/presscenter/news/20220815-11338.html

12 Daniel Nenni. 2022. "Ansys' Emergence as a Tier 1 EDA Player— and What That Means for 3D-IC". SemiWiki. https://semiwiki.com/eda/ansys-inc/318464-ansys-emergence-as-a-tier-1-eda-player-and-what-that-means-for-3d-ic/

13 Wally Rhines. 2019. "Chapter 7 – Competitive Dynamics in the Electronic Design Automation Industry." SemiWiki. https://semiwiki.com/wally-rhines/274440-chapter-7-competitive-dynamics-in-the-electronic-design-automation-industry/

14 Synopsys. 2022. "Strategic Acquisitions." https://www.synopsys.com/company/acquisitions.html

15 Synopsys. 2020. "Synopsys Collaborates with TSMC to Accelerate 3nm Innovation, Enabling Next-Generation SoC Design." https://news.synopsys.com/2020-08-25-Synopsys-Collaborates-with-TSMC-to-Accelerate-3nm-Innovation-Enabling-Next-Generation-SoC-Design

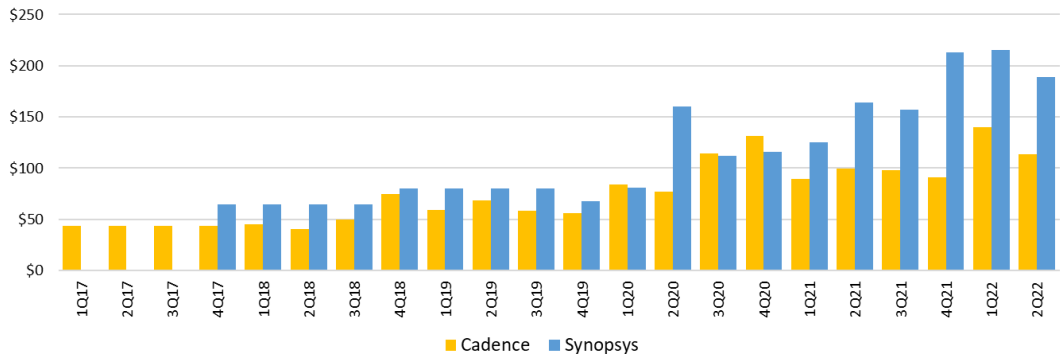
This necessarily extensive cooperation between EDA suppliers and foundries further incentivizes an oligopolistic market structure.

In summary, keeping these business dynamics of the EDA ecosystem in mind, it becomes clear why the EDA market is so consolidated and why it is so hard to compete with the "big three" at the cutting-edge. Importantly, these are challenges not just for China's EDA startups but also in part for open-source EDA initiatives. The next section will provide a brief overview of China's EDA ecosystem, focusing mainly on recent years.

China's rising EDA ecosystem

China's chip design ecosystem heavily depends on access to EDA tools from the three U.S. suppliers Synopsys, Cadence, and Mentor—just like the rest of the world. Previous analyses stated that the three leading U.S. EDA suppliers control 90 percent of China's EDA market.[16] Since Mentor was acquired by Siemens in 2017, no revenue data is publicly available. As for Cadence and Synopsys, Figure 1 shows their quarterly revenues within China.[17]

Figure 1: Cadence and Synopsys revenue in China in USD million
[source: company SEC filings]



[16] Douglas Fuller. 2020. "Cutting Off Our Nose to Spite Our Face: US Policy towards China in Key Semiconductor Industry Inputs, Capital Equipment and Electronic Design Automation Tools." https://ssrn.com/abstract=3672079 ; Elizabeth Xiao-Ru Wang, Sophie Yang, and Stephen Cacciola. 2020. "An Economic Analysis of the Effects of Stricter, Unilateral U.S. Export Controls for Electronic Design Automation Technology on Chinese Design." Compass Lexecon report commissioned by Cadence. https://downloads.regulations.gov/BIS-2021-0011-0040/attachment_2.pdf ; Jeff Pao. 2022. "EDA software ban latest blow to China's chip makers." https://asiatimes.com/2022/08/eda-software-ban-latest-blow-to-chinas-chip-makers/

[17] Cadence 1Q17-4Q17 is based on annual average; Synopsys FY ends in October, 4Q17–3Q19 are based on annual average.

For both companies, quarterly revenues tripled between Q1 2017 and Q1 2022 (see Figure 1). That said, even in Q1 2022 revenue from China only accounted for around 16 percent of total revenues from Cadence and Synopsys (see Figure 3). Thus, China is a quickly growing but not yet very dominant sales market for EDA suppliers. Knowing quarterly sales from Cadence and Synopsys and making some assumptions about Mentor's sales, one can reasonably **estimate that China's EDA market in 2021 was between $1.37 billion and $1.89 billion in revenue**. Below are the detailed calculations and underlying assumptions for upper (Table 1) and lower (Table 2) revenue bounds of China's EDA market.

Table 1: Upper revenue bound of China's EDA market in 2021: $1,888 million

Synopsys sales in China	$659.8 million[18]
Cadence sales in China	+ $378.2 million[19]
Mentor/Siemens EDA sales in China	+ *$472.4 million (estimated)*
	= $1,510.4 million (=80 percent)
	= $1,888 million (=100 percent)

Assumptions:

1. Synopsys, Cadence, and Mentor control **80 percent of China's EDA market**.
2. Mentor had **13 percent CAGR** from 2017–2021 (Synopsys and Cadence were at 11 percent):
   Mentor's revenue in 2016 was $1,282.5 million.[20] At 13 percent CAGR Mentor's 2021 revenue would be **$2,362 million**.
3. Mentor's **revenue share of China** grew from 14.7 percent in 2016 to 20 percent in 2021:
   1. 20 percent of $2,362 million is **$472.4 million**.

[18] Synopsys. 2022. SEC Filings (Form 10-Q). https://www.synopsys.com/company/investor-relations/annual-report.html

[19] Cadence. 2022. SEC Filings (Form 10-Q). https://www.cadence.com/en_US/home/company/investors/sec-filings.html

[20] Mentor Graphics. 2017. Annual Report. https://sec.report/Document/0000701811-17-000004/#s59A6F2DD31813549BA9DD55A585FB83B

Table 2: Lower revenue bound of China's EDA market in 2021: $1,372.5 million

Synopsys sales in China	$659.8 million
Cadence sales in China	+ $378.2 million
Mentor/Siemens EDA sales in China	+ *$197.3 million (estimated)*
	= $1,235.3 million (=90 percent) **= $1,372.5 million (=100 percent)**

Assumptions:

1. Synopsys, Cadence, and Mentor control **90 percent of China's EDA market**.
2. Mentor had **9 percent CAGR** from 2017–2021 (Synopsys and Cadence were at 11 percent):
   Mentor's revenue in 2016 was $1,282.5 million. At 9 percent CAGR Mentor's 2021 revenue would be **$1,973.3 million**.
3. Mentor's **revenue share of China** declined from 14.7 percent in 2016 to 10 percent in 2021:

   2. 10 percent of $1,973.3 million is **$197.3 million**.

Despite the dominant role that U.S. EDA suppliers are currently playing in China's chip design ecosystem, China's own EDA industry is rapidly growing, especially since 2020 with several initial public offerings (IPOs) and newly established startups from former Cadence and Synopsys executives. Cadence states in its 2021 annual report that there are "emerging competitors in China like Huada Empyrean, Xpeedic, X-EPIC, Primarius Technologies, and Giga-DA."[21] Following is a brief, non-exhaustive overview of Chinese EDA companies.

[21] Cadence. 2022. Form 10-K. https://d18rn0p25nwr6d.cloudfront.net/CIK-0000813672/2d2cec4c-acc6-4021-b698-259aec984cd2.pdf

Table 3: Public Chinese EDA Companies

Empyrean Technology[22] *Huada Jiutian*	Est.: **2009**, IPO: July 2022 (SSE: 301269) Revenue in 2021: **$84 million**, Employees: **687** Market capitalization August 2022: **$8.4 billion** Former subsidiary of China Electronics Corporation (CEC), merged in 2012 with ICScape (US)[23] Website: https://www.empyrean.com.cn/
Primarius Technologies[24] *Primarius*	Est.: **2010**, IPO: December 2021 (SSE: 688206) Revenue in 2021: **$28 million**, Employees: **239** Market capitalization August2022: **$2.4 billion** Founded by a former corporate vice president of Cadence[25] Roughly 50 percent of 2021 revenues were made outside of China[26] Website: https://www.khai-long.com/
Semitronix[27]	Est.: **2003**, IPO: August 2022 (SSE: 301095) Revenue in 2021: **$28.6 million**, Employees: **169** Market capitalization August 2022: **$2.87 billion** Website: http://www.semitronix.com/

[22] Google Finance. 2022. Empyrean Technology Co Ltd. https://www.google.com/finance/quote/301269:SHE

[23] Design & Reuse. 2012. "ICScape Grows Globally." https://www.design-reuse.com/news/29255/icscape-design-closure.html

[24] Google Finance. 2022. Primarius Technologies Co Ltd. https://www.google.com/finance/quote/688206:SHA

[25] Zhihong Liu. https://www.linkedin.com/in/zhihong-liu-82b63652/

[26] Li Panpan. 2022. "Chinese leading EDA company Primarius wins global giants Samsung, Micron, and TSMC as its clients." https://jw.ijiwei.com/n/824362

[27] Google Finance. 2022. Semitronix Corp. https://www.google.com/finance/quote/301095:SHE

Table 4: Chinese EDA startups

Hejian Industrial Software[28] *UniVista*	Est.: **2021**, by former president of Synopsys China[29] Total Funding: **>$404 million**, CN¥2.8 billion Investors: >**23 Chinese investors**, incl. National Integrated Circuit Industry Investment Fund[30] Employees[31]: **>300** Hejian tried to acquire the British EDA company Pulsic but the deal was blocked in August 2022 by the U.K. government on national security grounds[32] Website: https://www.univista-isg.com/
IC Bench[33] *Banxin Technologies*	Est.: **2020**, funding from Intel Capital, Lenovo Ventures, and others[34] Website: https://www.icbench.com/
X-EPIC	Est.: **2020**, by a former vice president of Synopsys China[35] and hired engineers from Cadence and Synopsys in leading positions[36] Total Funding[37]: **>$180 million** Website: https://www.x-epic.com/
Amedac *Advanced Manufacturing EDA Co.,Ltd*	Est.: **2019**, by a former vice president of Synopsys China[38] Total Funding: **>$14.5 million**, CN¥100 million

[28] Crunchbase. 2022. Hejian. https://www.crunchbase.com/organization/hejian

[29] Miranda Li. 2022. "Chinese EDA startup UniVista raised over RMB 1.1 billion in series pre-A round funding." https://jw.ijiwei.com/n/821269

[30] CBInsights. 2022. Hejian Industrial Software. https://app.cbinsights.com/profiles/c/zXrZO/overview

[31] The Paper. 2021. https://m.thepaper.cn/rss_newsDetail_15548442

[32] Jiaxing Li. 2022. "Shanghai software firm is behind Hong Kong's failed bid for UK's Pulsic, as geopolitics spurs rivalry for semiconductor supremacy." South China Morning Post. https://www.scmp.com/tech/big-tech/article/3189367/shanghai-software-firm-behind-hong-kongs-failed-bid-uks-pulsic

[33] Crunchbase. 2022. IC Bench. https://www.crunchbase.com/organization/ic-bench/

[34] Weixin. 2022. "Banxin Technology received Intel Capital Pre-A round of financing." https://mp.weixin.qq.com/s/Sx6w0cTrzuzHb0qvkBw5FQ

[35] Li Panpan. 2022. "Chinese EDA startup X-EPIC leads the industry with an EDA 2.0 concept of serving the entire system instead of chip design." https://jw.ijiwei.com/n/831272

[36] Che Pan. 2020. "Semiconductor software design start-up X-Epic secures US$30mn in new investment amid China's ongoing self-reliance drive." South China Morning Post. https://www.scmp.com/tech/start-ups/article/3113222/semiconductor-software-design-start-x-epic-secures-us30mn-new

[37] CBInsights. 2022. X-Epic. https://app.cbinsights.com/profiles/c/yZawr/overview

[38] Cheng Ting-Fang and Lauly Li. 2020. "China aims to shake US grip on chip design tools." https://asia.nikkei.com/Business/China-tech/China-aims-to-shake-US-grip-on-chip-design-tools

	Investors: **Joint venture with Synopsys (20 percent stake)**, Institute of Microelectronics Chinese Academy of Sciences and others[39] Website: https://www.amedac.com/
Giga-DA *Shenzhen Giga Design Automation Co., Ltd*	Est.: **2018**, emerged from the collapse of AtopTech (U.S.) and Avatar (U.S.) Funding: Shenzhen Hongtai Giga Investment Fund holds 90.91 percent equity of Giga; SMIT Group holds 9.09 percent[40] Website: http://www.giga-da.com/
Xpeedic Technology	Est.: **2010**, by a former Cadence employee[41] Total Funding[42]: **>$25 million** Employees: >100 Website: https://www.xpeedic.com/
S2C	Est.: **2003**, subsidiary of SmiT Group[43] Planned IPO was terminated in August 2022[44] Website: https://www.s2cinc.com/

This is just a small share of China's EDA industry. By some estimates there are currently more than 30 to 50 Chinese EDA companies[45]—from publicly traded companies such as Empyrean Technology with hundreds of employees (see Table 3) to newly established startups that raised a few million USD (see Table 4). Importantly, many of these startups were founded after 2018 when the U.S.-China technology rivalry intensified. **The three IPOs of Chinese EDA companies since 2021 and their high market capitalizations (see Table 3) are indicative of the fact that China's chip design ecosystem is actively looking for domestic alternatives.[46]**

[39] Peter Clarke. 2020. "China renews EDA effort with startup trio." https://www.eenewsanalog.com/en/china-renews-eda-effort-with-startup-trio/

[40] Giga-DA. 2021. "SMIT Group injected additional RMB90 million share capitals into Giga." http://www.giga-da.com/en/company3/52.html

[41] Crunchbase. 2022. Wenliang Dai. https://www.crunchbase.com/person/wenliang-dai-fa40

[42] Pitchbook. 2022. Xpeedic. https://pitchbook.com/profiles/company/265889-08#overview

[43] SMiT Group. https://www.smit.com.cn/en/profile.html

[44] Sohu. 2022. 国微思尔芯 IPO 被终止：曾拟募资 10 亿 君联与张江火炬为股东. https://www.sohu.com/a/573506509_430392

[45] Jeff Pao. 2022. "EDA software ban latest blow to China's chip makers." https://asiatimes.com/2022/08/eda-software-ban-latest-blow-to-chinas-chip-makers/ ; The Paper. 2021. https://m.thepaper.cn/rss_newsDetail_15548442

[46] Cheng Ting-Fang and Lauly Li. 2021. "US-China tech war: Beijing's secret chipmaking champions." https://asia.nikkei.com/Spotlight/Most-read-in-2021/US-China-tech-war-Beijing-s-secret-chipmaking-champions

But Chinese EDA companies are not just focused on the domestic market: 50 percent of Primarius' revenue in 2021 was from foreign customers. Empyrean, Giga-DA, Phlexing, Primarius, Semitronix, and Xpeedic are official partners of Samsung's foundry program.[47] Amedac, Empyrean, Primarius, S2C, and Xpeedic are members of Semiconductor Equipment and Materials International's (SEMI) global Electronic System Design Alliance.[48] Empyrean is also in TSMC's EDA Alliance[49] and the Silicon Integration Initiative (a U.S.-based global industry consortium to advance EDA capabilities).[50] Chinese EDA suppliers are also increasingly participating in some of the leading international EDA conferences, such as the prestigious Design Automation Conference.[51] Of course, many of the newly established startups will fail and even Empyrean, the largest EDA supplier in China, only has a complete design flow for analog semiconductors and hopes to offer one for cutting-edge logic chips by 2030.[52] That said, not all of these companies aim to compete with Cadence and Synopsys by offering a complete design flow but instead focus on specific design steps. One example would be S2C that offers globally competitive hardware-based prototyping solutions.[53] **This goes to show that besides the United States, China currently has the most active and fastest moving EDA ecosystem.**

A virtuous cycle: Chinese EDA suppliers, foundries, and chip design

Chinese EDA companies, and by extension Chinese chip design companies, can count on an increasingly competitive domestic foundry landscape. This is relevant because of the necessarily close collaboration between foundries and EDA suppliers. Assuming that Chinese foundries would be even more willing than foreign foundries to collaborate with (currently inferior) Chinese EDA suppliers, an increasingly capable Chinese foundry landscape also empowers Chinese EDA suppliers. While recent news about Semiconductor Manufacturing International Corporation (SMIC), China's most competitive foundry and fifth largest globally by revenue, being able to manufacture 7

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47 Samsung. 2022. Samsung Advanced Foundry Ecosystem. https://semiconductor.samsung.com/foundry/safe/eda/

48 ESD Alliance. 2022. https://www.semi.org/en/communities/esda/membership-directory

49 TSMC. 2022. EDA Alliance. https://www.tsmc.com/english/dedicatedFoundry/oip/eda_alliance

50 Silicon Integration Initiative. 2022. https://si2.org/

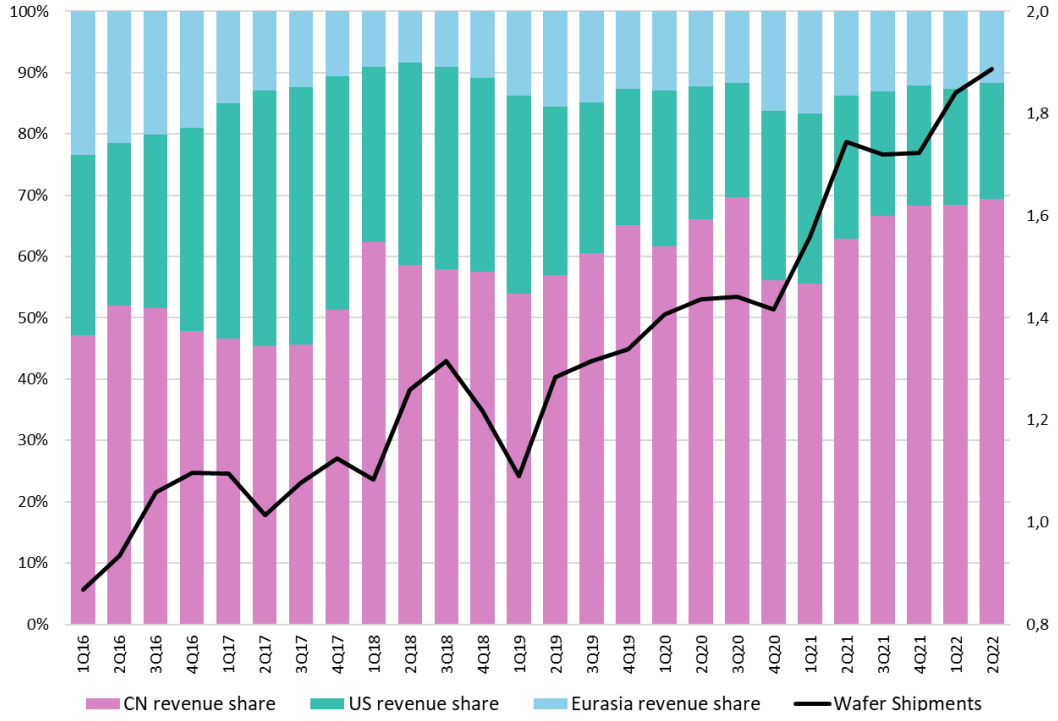
51 Design Automation Conference. 2022. https://www.dac.com/About/Conference-Archive ; The Paper. 2021. https://m.thepaper.cn/baijiahao_15343112

52 Elizabeth Xiao-Ru Wang, Sophie Yang, and Stephen Cacciola. 2020. "An Economic Analysis of the Effects of Stricter, Unilateral U.S. Export Controls for Electronic Design Automation Technology on Chinese Design." Compass Lexecon report commissioned by Cadence. https://downloads.regulations.gov/BIS-2021-0011-0040/attachment_2.pdf

53 SemiWiki. 2021. "S2C EDA Delivers on Plan to Scale-Up FPGA Prototyping Platforms to Billions of Gates." https://semiwiki.com/prototyping/s2c-eda/304634-s2c-delivers-on-plan-to-scale-up-fpga-prototyping-platforms-to-billions-of-gates/

nm chips received a lot of attention from policymakers,[54] it is equally interesting that over the past five years SMIC changed from a foundry mainly serving foreign customers to one that predominantly manufactures chips for customers in China: **Figure 2** shows the quarterly share of SMIC's revenue from Chinese, U.S., and Eurasian customers (left side, in percent) and SMIC's total number of shipped wafers per quarter (black line, right side in millions of wafers).

Figure 2: SMIC regional revenue (left), wafer shipments (right, in millions of wafers [source: quarterly reports]



Between 2016 and 2022 SMIC's revenue share of Chinese customers grew significantly, and China's largest foundry was able to double its wafer output at the same time.

- **H1 2016**: Chinese customers accounted for less than 50 percent of SMICs revenue and around 896,000 shipped wafers.
- **H1 2022:** Chinese customers were responsible for close to 70 percent of SMIC's revenue and around 2,568,000 shipped wafers.

[54] Scotten Jones. 2022. "Does SMIC have 7nm and if so, what does it mean." SemiWiki. https://semiwiki.com/semiconductor-services/ic-knowledge/317732-does-smic-have-7nm-and-if-so-what-does-it-mean/

Chinese EDA suppliers can benefit from this virtuous cycle: With an increasingly competitive foundry ecosystem in China and a supposed willingness of Chinese foundries to cooperate with Chinese EDA suppliers, chip design companies might be more willing to switch to Chinese EDA tools at least for trailing-edge and advanced nodes, if not for cutting-edge process nodes.

That said, the newest U.S. export controls from October 7, 2022, intend to cut off Chinese fabs from cutting-edge manufacturing technology, "freezing" their capabilities at trailing-edge levels (>14 nm).[55] This in turn means that Chinese EDA suppliers need to cooperate with TSMC in Taiwan or Samsung in Korea to develop EDA toolchains at below 14 nm, which could be easily restricted by the U.S. government. This makes it extremely hard for China's EDA suppliers to catch up to the cutting-edge and compete internationally. Chinese EDA suppliers will certainly continue to compete in various other semiconductor categories, such as analog chips or power semiconductors, but they will be hard pressed to develop a complete toolchain necessary to design cutting-edge logic semiconductors, such as mobile chipsets, AI accelerators, or server processors.

In summary: China's EDA ecosystem will grow, but not at the cutting-edge

In summary, China's EDA ecosystem cannot compete with the dominant U.S. EDA suppliers in the short or medium term. Chinese chip design companies, especially for cutting-edge logic chips (e.g., AI accelerators, mobile chipsets, server- and desktop-processors), will continue to heavily rely on U.S. EDA suppliers within this decade. That said, China's semiconductor ecosystem has all the ingredients to substantially strengthen its domestic EDA suppliers in the long term: a quickly advancing chip design ecosystem with companies such as Alibaba, Baidu, BYD, Tencent, and Xiaomi, all developing their own chips, an increasingly competitive foundry ecosystem at least for trailing-edge and mature manufacturing processes, and public and private venture capital eager to invest in domestic EDA companies.

In fact, if it was just about curbing the technological advancements of China's chip design ecosystem, controlling the export of EDA tools capable to design chips based on the next transistor generation (GAAFET), as was agreed in December 2021 among the member states of the Wassenaar Arrangement, would most likely be enough. After all, China is responsible for just around 15 percent of Cadence's and Synopsys's revenues (Figure 3), significantly less than China's revenue shares at some U.S. semiconductor manufacturing equipment suppliers who generate more than 30 percent of revenues from customers in China.

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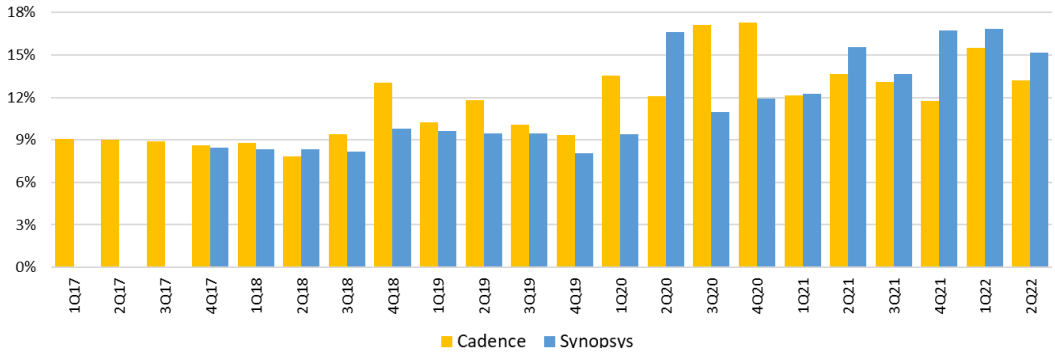
[55] Reva Goujon, Lauren Dudley, Jan-Peter Kleinhans, and Agatha Kratz. 2022. "Freeze-in-Place: The Impact of US Tech Controls on China". Rhodium Group. https://rhg.com/research/freeze-in-place/

Figure 3: Cadence and Synopsys share of revenue from Chinese customers [source: company SEC filings]



But a policy strategy solely focused on controlling the export of cutting-edge EDA tools to China as well as freezing China's foundry ecosystem at trailing-edge levels would only "protect" the U.S. and allied governments from Chinese competition in the short to medium term. It would need to be complemented by a "promote" strategy focused not just on a single technology but on the long-term competitiveness of the innovation ecosystem itself.[56] Incentivizing the development and adoption of open-source EDA tools would constitute such a "promote" strategy. The next section explains why the trend toward open-source EDA tools as well as open-source process development kits by foundries creates an opportunity to significantly lower the barriers to entry to chip design ("democratizing chip design"). Importantly, government incentives to strengthen the open-source EDA ecosystem would not necessarily weaken the oligopoly of U.S. suppliers for EDA tools necessary to design cutting-edge chips. This, in turn, means that the U.S. government could use export controls on cutting-edge EDA tools while, at the same time, support the development of an open-source EDA ecosystem for trailing-edge and mature nodes.

Open-source EDA to promote long-term competitiveness

While EDA tools and manufacturing equipment are both mere inputs—supplier markets—within the semiconductor industry, they have fundamentally different dynamics with direct implications for policymakers. Semiconductor manufacturing equipment vendors, especially for cutting-edge equipment, have relatively few customers because not many companies can afford to build fabs that cost $10 billion or

[56] Owen Daniels and Will Hunt. 2022. "Sustaining and Growing the U.S. Semiconductor Advantage: A Primer". https://cset.georgetown.edu/publication/sustaining-and-growing-the-u-s-semiconductor-advantage-a-primer/

more. Even trailing-edge fabs for analog or power semiconductors, that are significantly "cheaper," have steep market entry barriers and there are simply not many companies with the necessary skills and money. This is in stark contrast to the market dynamics within EDA and their customers: Many more companies are designing their own silicon than running their own fabs. There is not just an increasing amount of chip design startups worldwide but also many established companies in different sectors started designing their own chips in recent years—from Amazon to BMW, Google, and Tesla. The reason for that is twofold: (1) For many areas, such as machine learning or traffic management in data centers, general-purpose processors are simply not efficient enough anymore[57]; (2) by designing their own chips companies can gain a competitive advantage and raise market-entry barriers for everybody else.[58] Thus, while there are only a handful of companies with cutting-edge logic fabs (TSMC Samsung, Intel), there are countless companies designing their own chips—with the help of EDA tools.

EDA can be understood as an enabling "platform" technology. The easier it is (in terms of financial and human resources) to design a chip, and the more capable EDA tools are, the more they empower a thriving chip design ecosystem. Lowering these barriers to design chips is not just relevant to spur innovation in academic research but also to enable chip design in sectors that simply do not have the economies of scale and chip volumes that information and communication technologies or automotive industries have, such as the military, agriculture, or medical devices. There is a growing community of researchers (from academia and the government, including the military), startups, and companies designing chips that argue that the lack of open-source EDA tools hinders innovation in chip design.

> *Commercial electronic design automation (EDA) tools have become extremely complex as they evolve to meet the demands of design organizations who create products in leading-edge technology nodes and whose goal is to hyper optimize their designs with significant manual effort. Today, EDA tool and design process outcomes are difficult to predict, and expert tool users are needed. This raises barriers of cost, expertise, and risk to hardware innovation.*[59]

The DARPA, as part of its Electronics Resurgence Initiative, substantially invested in the development of open-source EDA tools, through projects such as OpenROAD.[60]

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[57] Neil Thompson and Svenja Spanuth. 2018. "The Decline of Computers As a General Purpose Technology: Why Deep Learning and the End of Moore's Law are Fragmenting Computing." https://ssrn.com/abstract=3287769

[58] Digits to Dollars. 2021. "Let's Build a Chip – With Math." https://digitstodollars.com/2021/05/28/lets-build-a-chip-with-math/

[59] Andrew B. Kahng and Tom Spyrou. 2021. "The OpenROAD Project: Unleashing Hardware Innovation." https://vlsicad.ucsd.edu/Publications/Conferences/374/c374.pdf

[60] OpenROAD. 2022. https://theopenroadproject.org/about-us/

The goal is to develop an open-source EDA toolchain to lower the barriers to chip design. Importantly, OpenROAD and other DARPA initiatives, aiming at innovation in chip design, speak to the fact that the U.S. Department of Defense is worried about its long-term ability to develop and design chips, not just for direct national security purposes but also to ensure U.S. technology leadership—using open-source tools. Since its start in 2018 OpenROAD has been highly successful and coincided with other open-source initiatives within the chip design ecosystem.[61]

- **RISC-V**, an open instruction set architecture (ISA), has received substantial attention from both industry and academics,[62] including many Chinese companies. An ISA defines the fundamental commands (set of instructions) a processor works on. Historically these ISAs have been proprietary, such as Intel's x86 or the ARM from Arm Holdings. As an open-source ISA, RISC-V established an alternative to the existing incumbents. Importantly, an open-source ISA has nothing to do with open-source EDAs and many, if not most, processor cores developed based on RISC-V are proprietary.
- **Open Process Development Kits (PDKs)**: PDKs hold essential information for chip designers as they define the physical characteristics of the manufacturing process a chip will be based on. PDKs are typically not open sourced and can only be accessed through non-disclosure agreements. Google, together with the U.S.-based foundry SkyWater Technology (SkyWater) and the chip design platform Efabless released an **open PDK for SkyWater 130 nm process node** in 2020. Due to sponsorship from Google, chip designers were able to produce limited amounts of chips free of charge through the Efabless platform.[63] In summer 2022, through the same Google collaboration, an open PDK for **SkyWater 90 nm process**[64] as well as **GlobalFoundries 180 nm process** were announced.[65] In September 2022 Google and the U.S. National Institute of Standards and Technology (NIST) announced a cooperation "to develop an open source testbed for nanotechnology research and development."[66]

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61 Tom Spyrou. 2022. "OpenROAD 3 Years in Perspective." https://open-source-eda-birds-of-a-feather.github.io/doc/slides/DAC2022%20birds%20of%20a%20feather%20open%20source%20EDA.pdf

62 Brian Bailey. 2022. "Why RISC-V Is Succeeding." https://semiengineering.com/why-risc-v-is-succeeding/

63 efabless. 2022. Open Shuttle Program. https://efabless.com/open_shuttle_program

64 Google Open Source Blog. 2022. "SkyWater and Google expand open source program to new 90nm technology." https://opensource.googleblog.com/2022/07/SkyWater-and-Google-expand-open-source-program-to-new-90nm-technology.html

65 Google Open Source Blog. 2022. "GlobalFoundries joins Google's open source silicon initiative." https://opensource.googleblog.com/2022/08/GlobalFoundries-joins-Googles-open-source-silicon-initiative.html

66 Google Open Source Blog. 2022. "Google and NIST partner on nanotechnology development platform". https://opensource.googleblog.com/2022/09/google-and-nist-partner-on-nanotechnology-development-platform.html

Designing a 90 nm chip with an open-source EDA toolchain seems negligible, maybe even foolish, in a global ecosystem that is ramping up production of 3 nm chips with tens of billions of transistors. Yet, if nothing else, Google is not heavily investing in open silicon for the fun of it. The world has an insatiable hunger for compute power in a time when (a) Moore's Law is either dead or at least substantially slowing down, (b) the shortage of hardware engineers is worsening while (c) companies are in dire need of application-specific chips because of (a).[67] Enabling more people to design hardware by lowering the barriers to entry through open-source EDA tools, open-source PDKs, and open-source IP makes economic sense, at least for a hyperscaler like Google.

The potential long-term trend of "open silicon" (open-source EDA, IP, PDK) is the reason why controlling the export of cutting-edge EDA tools to China needs to be complemented by a long-term strategy to "promote" the development of an open-source EDA ecosystem at the trailing-edge. Restricting China's access to proprietary, cutting-edge EDA software should not preclude policymakers from continued investments in an open EDA ecosystem. At least within this decade it is highly unlikely that (a) open-source EDA tools will reach the maturity of their proprietary counterparts, (b) that foundries will release open-source PDKs of their cutting-edge process nodes, and that (c) a plethora of competitive open-source IP blocks is available. Open EDA will most-likely coexist with proprietary solutions as they serve different needs. Parallels can be drawn to software, where the Windows operating system is indispensable to desktops and laptops but around 80 percent of Internet servers are using Linux.[68]

> *Well, working for Cadence, it has not escaped my notice that the success of this project might be a threat to Cadence's business, certainly with the existing business model. Linux was laughed off as being just a 'bunch of volunteers' but its success has been almost total in the server and supercomputer space… Even if this project only succeeds for non-leading-edge designs… it could still be a commercial threat by draining off a lot of revenue.*[69]

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[67] Tim Ansell and Mehdi Saligane. 2022. "The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts." Google. https://dl.acm.org/doi/pdf/10.1145/3400302.3415736

[68] W3Techs. 2022. "Usage statistics of operating systems for websites." https://w3techs.com/technologies/overview/operating_system

[69] Breakfast Bytes Blog. 2018. "ERI: OpenROAD." Cadence. https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/darpa-and-open-source

No chokepoints without oligopolies

Restrictive policies, such as export controls or investment screening, always have a forward- and backward-looking aspect. They are forward-looking in their assessment of how a product or technology acquisition might strengthen China's capabilities in a specific domain. They are backward-looking because they assess the current situation in a technology ecosystem in terms of market structure, barriers to entry, substitutability, military utility, and much more. At the nexus of U.S.-China technology competition, chip design, and EDA, some forecasts can be made with relative certainty:

- China's chip design ecosystem will grow and most likely be able to compete internationally.[70]
- Chinese EDA tool suppliers will be able to capitalize on that and gain market shares from Cadence, Mentor, and Synopsys, for design of trailing-edge chips and specific steps in the design flow.
- Within this decade it is highly unlikely that a Chinese EDA tool supplier will be able to meaningfully compete with Cadence, Mentor, and Synopsys in complete design flows for cutting-edge logic chips.

Until now the EDA industry, from a policymaker's perspective, seems very similar to that of manufacturing equipment: Deny China access to cutting-edge EDA tools to curb its technological advancements. But such a "protect" strategy should be complemented by a "promote" strategy, focused on the long-term potential of an open-source EDA ecosystem. An oligopoly of proprietary EDA tools for cutting-edge chip designs can co-exist with freely available EDA tools that significantly lower the barriers to entry for chip designs at the trailing-edge and mature nodes.

Especially when considering long-term economic dynamics (increasing complexity of and barriers to chip design, lack of hardware versus software engineers) as well as the potential national security dimension (the military's ability to develop application-specific chips), the value proposition of open-source EDA tools seems to make sense. When policymakers are confronted with the dilemma of controlling China's access to EDA tools and, at the same time, incentivizing the development of open-source EDA tools, policies should be shaped by a forward-looking agenda: The competition is not in a single technology but on the level of technology ecosystems and the capacity to innovate. Openness sparks innovation.

[70] ServeTheHome. 2022. "Biren BR100 GPU for Datacenter Compute and AI Workloads." https://www.servethehome.com/biren-br100-gpu-for-datacenter-compute-and-ai-workloads/